Abstract

[0046] A phase lock loop lock detect circuit determines whether an output signal of the phase lock loop is in phase-frequency synchronization with an input reference timing signal and provides an unlock alarm signal indicating that the output signal of a phase lock loop is no longer in phase-frequency synchronization with an input reference timing signal. The lock detection circuit has a first logic function circuit to combine a frequency increase signal and a frequency decrease signal of said phase lock loop to provide a frequency deviation signal. The first logic function in the preferred embodiment of this invention is an OR gate. The output of the first logic function circuit is an input to a second logic function circuit. The second logic function circuit combines the frequency deviation signal with the input reference signal, which is applied to a second input of the second logic function, to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said input reference signal and provide an unlock alarm signal. The second logic function circuit in the preferred embodiment of this invention is an AND gate. The lock detection circuit further includes a latching circuit in communication with the second logic function and the input reference signal to capture and retain said unlock alarm signal indicating loss of phase-frequency lock of said phase lock loop.